REMARKS

The indication of allowable subject matter in claims 6, 7, and 14 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 1 and 15 are independent and stand rejected under 35 U.S.C. § 103 as being unpatentable over Applicants' admitted prior art ("APA") in view of Farnworth et al. '087 ("Farnworth"). This rejection is respectfully traversed for the following reasons.

Claims 1 and 15 each embody a step of bonding a surface protection tape ***to the wafer*** using an adhesive material which contacts the passivation film. The Examiner admits that APA does not disclose that the alleged adhesive material 320 contacts the alleged passivation film 306 (*see, e.g.,* Figure 21B of Applicants' drawings). The Examiner therefore relies on Farnworth as allegedly disclosing an adhesive material 52 which contacts a passivation film 50 formed above an alleged wafer 32. However, it is respectfully submitted that Farnworth is directed to the structure of a packaged die 32 that has been separated from the wafer 30, so that the teachings thereof are completely unrelated to the structure of APA shown in Figure 21B of Applicants' drawings which the Examiner attempts to modify.

Specifically, the alleged adhesive material 52 is not bonded ***to the wafer 30*** of Farnworth in the manner specified in the present invention (*see* Figure 2A of Farnworth). Rather, the alleged adhesive material 52 is bonded ***to die 32***, which has been cut out from the wafer 30 (*see* col. 4, lines 38-41 of Farnworth). Accordingly, the relied on teachings of Farnworth are, at best, relevant to APA for the processing performed ***after*** the polishing process for the wafer 302 and after the chips are cut out from the wafer 302. That is, the relied on teachings of Farnworth

shown in Figure 4 thereof do NOT correspond to the wafer processing shown in Figure 21B of APA which the Examiner attempts to modify, but instead relate to after polishing the wafer and the chip is cut away from the wafer. The proposed combination does not suggest a step of bonding a surface protection tape ***to the wafer prior to a polishing step***.

Indeed, one of the features of the present invention is directed to the ***wafer polishing*** process in that the step of bonding the surface protection tape to the wafer, whereby an adhesive material contacts the passivation film in the whole periphery region of the wafer, can prevent the polishing slurry from permeating into the inside in the subsequent rear surface polishing step. The alleged adhesive material 52 of Farnworth is illustrated as part of the cut away chip 32 so that Farnworth does not suggest polishing the rear surface of the wafer after the alleged adhesive material 52 is bonded to the die 32 and is in fact unrelated to such processing, and there is no motivation to apply the adhesive 52 of Farnworth ***to the wafer 302 of APA prior to a polishing step***.

Moreover, the Examiner's motivation for making the proposed combination further evidences the irrelevance of the die structure 32 to the wafer 302 processing of APA. Specifically, the Examiner alleges that the proposed combination would have been obvious "to provide separate electrical paths between the solder bumps and flex circuit conductors." However, this motivation is related to a die structure 32 that has been cut away from a wafer, and is not related to the wafer 302 polishing process of APA in which the chips have not yet been separated from the wafer.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 1 and 15 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1 and 15 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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